



High-Performance, Fully-Differential AUDIO OP AMP

FEATURES

- SUPERIOR SOUND QUALITY
- ULTRA LOW DISTORTION: 0.000022%
- LOW NOISE: $1.3\text{nV}/\sqrt{\text{Hz}}$
- HIGH SPEED:
 - Slew Rate: $50\text{V}/\mu\text{s}$
 - Gain Bandwidth: 180MHz
- FULLY DIFFERENTIAL ARCHITECTURE:
 - Balanced Input and Output Converts Single-Ended Input to Balanced Differential Output
- WIDE SUPPLY RANGE: $\pm 2.5\text{V}$ to $\pm 16\text{V}$
- SHUTDOWN TO CONSERVE POWER

APPLICATIONS

- AUDIO ADC DRIVER
- BALANCED LINE DRIVER
- BALANCED RECEIVER
- ACTIVE FILTER
- PREAMPLIFIER

DESCRIPTION

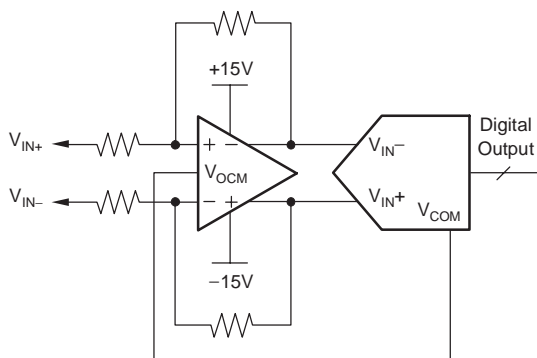
The OPA1632 is a fully-differential amplifier designed for driving high-performance audio analog-to-digital converters (ADCs). It provides the highest audio quality, with very low noise and output drive characteristics optimized for this application. The OPA1632's excellent gain bandwidth of 180MHz and very fast slew rate of $50\text{V}/\mu\text{s}$ produce exceptionally low distortion. Very low input noise of $1.3\text{nV}/\sqrt{\text{Hz}}$ further ensures maximum signal-to-noise ratio and dynamic range.

The flexibility of the fully differential architecture allows for easy implementation of a single-ended to fully-differential output conversion. Differential output reduces even-order harmonics and minimizes common-mode noise interference. The OPA1632 provides excellent performance when used to drive high-performance audio ADCs such as the PCM1804. A shutdown feature also enhances the flexibility of this amplifier.

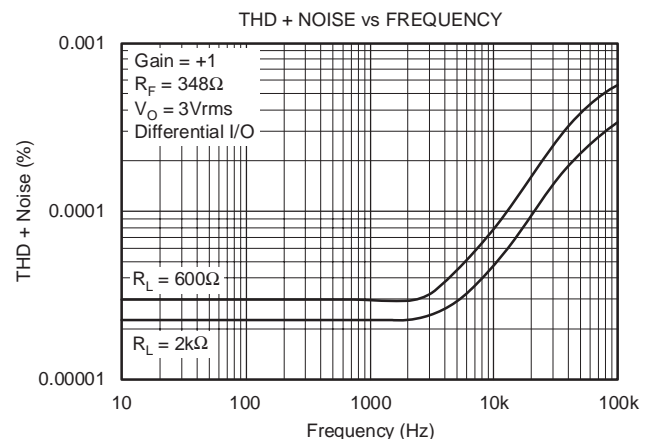
The OPA1632 is available in an SO-8 package and a thermally-enhanced MSOP-8 PowerPAD™ package.

RELATED DEVICES

OPAx134	High-Performance Audio Amplifiers
OPA627/637	Precision High-Speed DiFET Amplifiers
OPAx227/x228	Low-Noise Bipolar Amplifiers



Typical ADC Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DRAWING	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA1632	SO-8	D	-40°C to +85°C	OPA1632	OPA1632D	Rails, 100
					OPA1632DR	Tape and Reel, 2500
	MSOP-8 PowerPAD	DGN	-40°C to +85°C	1632	OPA1632DGN	Rails, 100
					OPA1632DGNR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range unless otherwise noted.

Supply Voltage, $\pm V_S$	$\pm 16.5V$
Input Voltage, V_I	$\pm V_S$
Output Current, I_O	150mA
Differential Input Voltage, V_{ID}	$\pm 3V$
Maximum Junction Temperature, T_J	150°C
Operating Free-Air Temperature Range	-40°C to +85°C
Storage Temperature Range, T_{STG}	-65°C to +150°C
ESD Ratings: Human Body Model	1kV
Charge Device Model	500V
Machine Model	200V

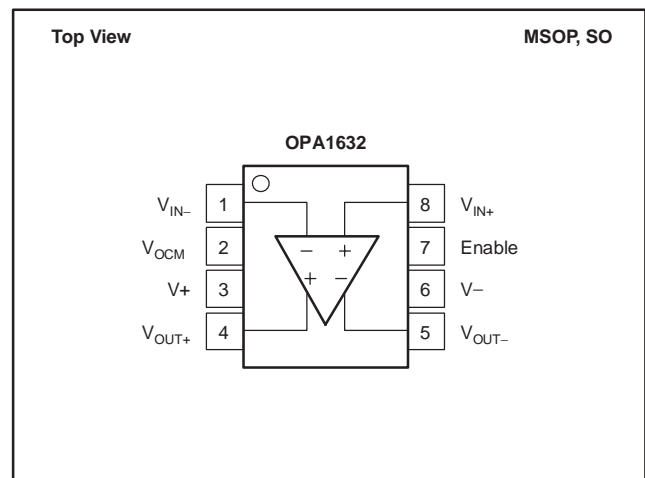
- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The OPA1632 MSOP-8 package version incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature, which can permanently damage the device. See TI technical brief SLMA002 for more information about using the PowerPAD thermally enhanced package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS: $V_S = \pm 15V$

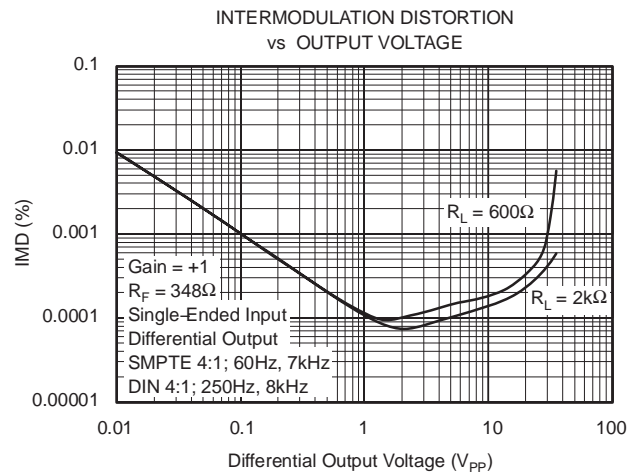
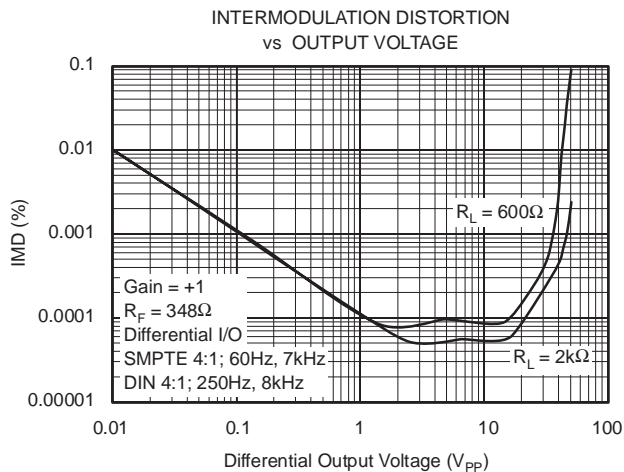
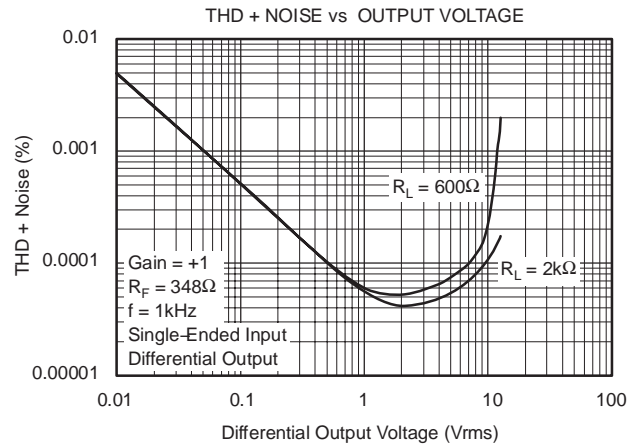
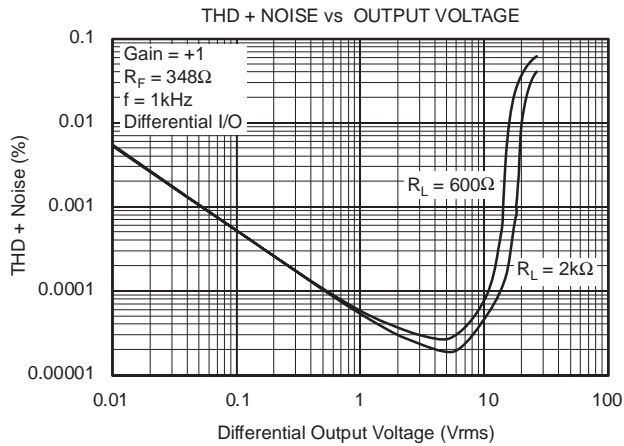
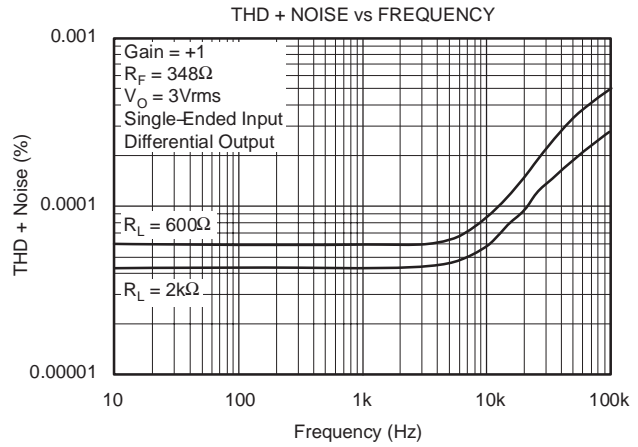
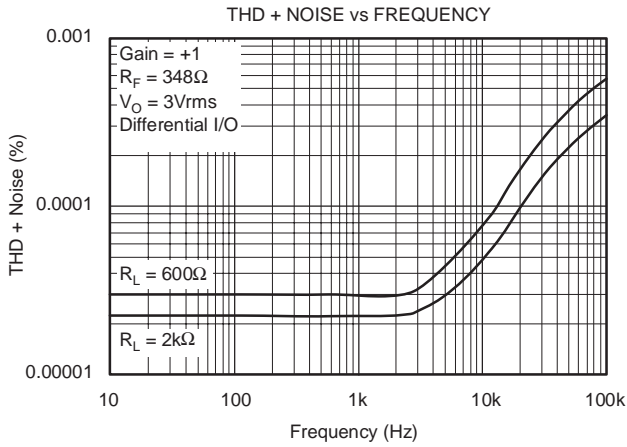
$V_S = \pm 15V$: $R_F = 390\Omega$, $R_L = 800\Omega$, and $G = +1$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA1632			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage			± 0.5	± 3	mV
vs Temperature	dVos/dT		± 5		$\mu V/^\circ C$
vs Power Supply, DC	PSRR	316	13		$\mu V/V$
INPUT BIAS CURRENT					
Input Bias Current	I_B		2	6	μA
Input Offset Current	I_{OS}		± 100	± 500	nA
NOISE					
Input Voltage Noise	f = 10 kHz		1.3		nV/\sqrt{Hz}
Input Current Noise	f = 10 kHz		0.4		pA/\sqrt{Hz}
INPUT VOLTAGE					
Common-Mode Input Range		$(V-) + 1.5$		$(V+) - 1$	V
Common-Mode Rejection Ratio, DC		74	90		dB
INPUT IMPEDANCE					
Input Impedance (each input pin)			34 4		$M\Omega pF$
OPEN-LOOP GAIN					
Open-Loop Gain, DC		66	78		dB
FREQUENCY RESPONSE					
Small-Signal Bandwidth	G = +1, $R_F = 348\Omega$		180		MHz
	G = +2, $R_F = 602\Omega$		90		MHz
	G = +5, $R_F = 1.5k\Omega$		36		MHz
	G = +10, $R_F = 3.01k\Omega$		18		MHz
Bandwidth for 0.1dB Flatness	G = +1, $V_O = 100mV_{pp}$		40		MHz
Peaking at a Gain of 1	$V_O = 100mV_{pp}$		0.5		dB
Large-Signal Bandwidth	G = +2, $V_O = 20V_{pp}$		800		kHz
Slew Rate (25% to 75%)	G = +1		50		V/ μs
Rise and Fall Time	G = +1, $V_O = 5V$ Step		100		ns
Settling Time to 0.1%	G = +1, $V_O = 2V$ Step		75		ns
0.01%	G = +1, $V_O = 2V$ Step		200		ns
Total Harmonic Distortion + Noise	G = +1, f = 1kHz, $V_O = 3V_{rms}$				
Differential Input/Output	$R_L = 600\Omega$		0.0003		%
Differential Input/Output	$R_L = 2k\Omega$		0.000022		%
Single-Ended In/Differential Out	$R_L = 600\Omega$		0.000059		%
Single-Ended In/Differential Out	$R_L = 2k\Omega$		0.000043		%
Intermodulation Distortion	G = +1, SMPTE/DIN, $V_O = 2V_{pp}$				
Differential Input/Output	$R_L = 600\Omega$		0.00008		%
Differential Input/Output	$R_L = 2k\Omega$		0.00005		%
Single-Ended In/Differential Out	$R_L = 600\Omega$		0.0001		%
Single-Ended In/Differential Out	$R_L = 2k\Omega$		0.0007		%
Headroom	THD < 0.01%, $R_L = 2k\Omega$		20.0		V _{pp}
OUTPUT					
Voltage Output Swing	$R_L = 2k\Omega$	$(V+) - 1.9$		$(V-) + 1.9$	V
	$R_L = 800\Omega$	$(V+) - 4.5$		$(V-) + 4.5$	V
Short-Circuit Current	Sourcing/Sinking	+50/-60	85		mA
Closed-Loop Output Impedance	G = +1, f = 100kHz		0.3		Ω
POWER-DOWN⁽¹⁾					
Enable Voltage Threshold			$(V-) + 2$		V
Disable Voltage Threshold			$(V-) + 0.8$		V
Shutdown Current	$V_{ENABLE} = -15V$		0.85	1.5	mA
Turn-On Delay	Time for I_Q to Reach 50%		2		μs
Turn-Off Delay	Time for I_Q to Reach 50%		2		μs
POWER SUPPLY					
Specified Operating Voltage			± 15	± 16	V
Operating Voltage		± 2.5			V
Quiescent Current	I_Q Per Channel		14	17.1	mA
TEMPERATURE RANGE					
Specified Range		-40		+85	$^\circ C$
Operating Range		-40		+125	$^\circ C$
Storage Range		-65		+150	$^\circ C$
Thermal Resistance	θ_{JA}		200		$^\circ C/W$

(1) Amplifier has internal 50k Ω pull-up resistor to V_{CC+} pin. This enables the amplifier with no connection to shutdown pin.

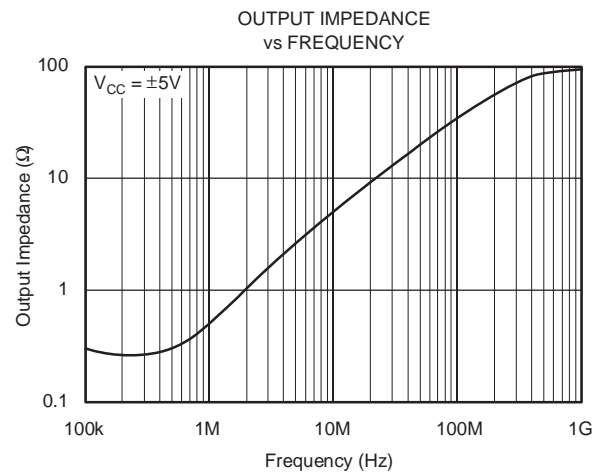
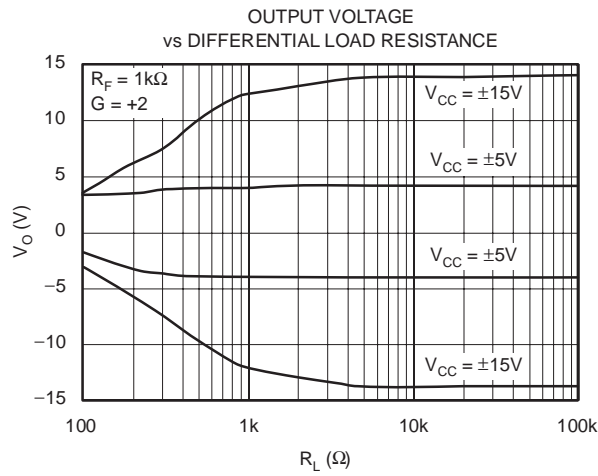
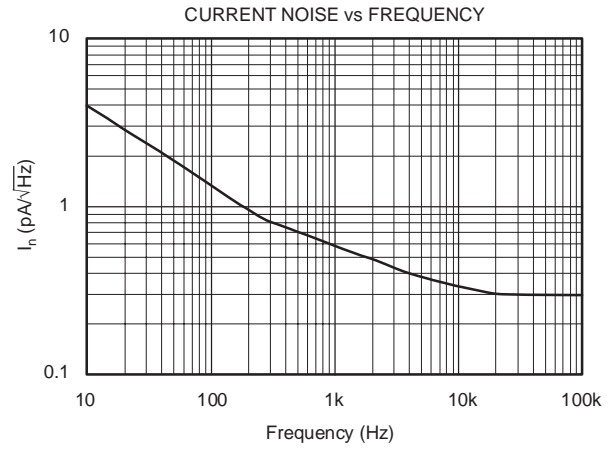
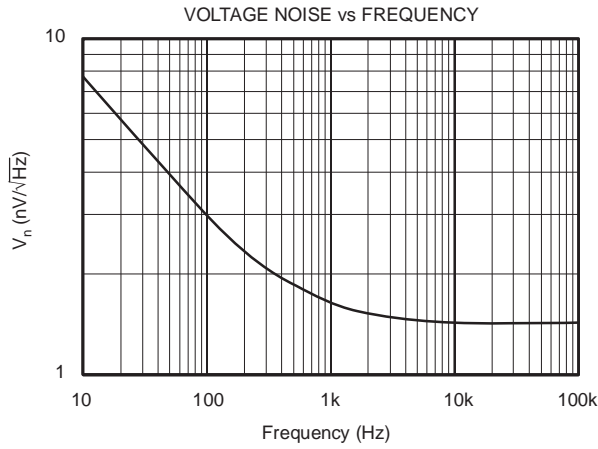
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 2\text{k}\Omega$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 2\text{k}\Omega$, unless otherwise noted.



APPLICATIONS INFORMATION

Figure 1 shows the OPA1632 used as a differential-output driver for the PCM1804 high-performance audio ADC.

Supply voltages of $\pm 15\text{V}$ are commonly used for the OPA1632. The relatively low input voltage swing required by the ADC allows use of lower power-supply voltage, if desired. Power supplies as low as $\pm 8\text{V}$ can be used in this application with excellent performance. This reduces power dissipation and heat rise. Power supplies should be bypassed with $10\mu\text{F}$ tantalum capacitors in parallel with $0.1\mu\text{F}$ ceramic capacitors to avoid possible oscillations and instability.

The V_{COM} reference voltage output on the PCM1804 ADC provides the proper input common-mode reference voltage (2.5V). This V_{COM} voltage is buffered with op amp A_2 and drives the output common-mode voltage pin of the OPA1632. This biases the average output voltage of the OPA1632 to 2.5V .

The signal gain of the circuit is generally set to approximately 0.25 to be compatible with commonly-used audio line levels. Gain can be adjusted, if necessary, by

changing the values of R_1 and R_2 . The feedback resistor values (R_3 and R_4) should be kept relatively low, as indicated, for best noise performance.

R_5 , R_6 , and C_3 provide an input filter and charge glitch reservoir for the ADC. The values shown are generally satisfactory. Some adjustment of the values may help optimize performance with different ADCs.

It is important to maintain accurate resistor matching on R_1/R_2 and R_3/R_4 to achieve good differential signal balance. Use 1% resistors for highest performance. When connected for single-ended inputs (inverting input grounded, as shown in Figure 1), the source impedance must be low. Differential input sources must have well-balanced or low source impedance.

Capacitors C_1 , C_2 , and C_3 should be chosen carefully for good distortion performance. Polystyrene, polypropylene, NPO ceramic, and mica types are generally excellent. Polyester and high-K ceramic types such as Z5U can create distortion.

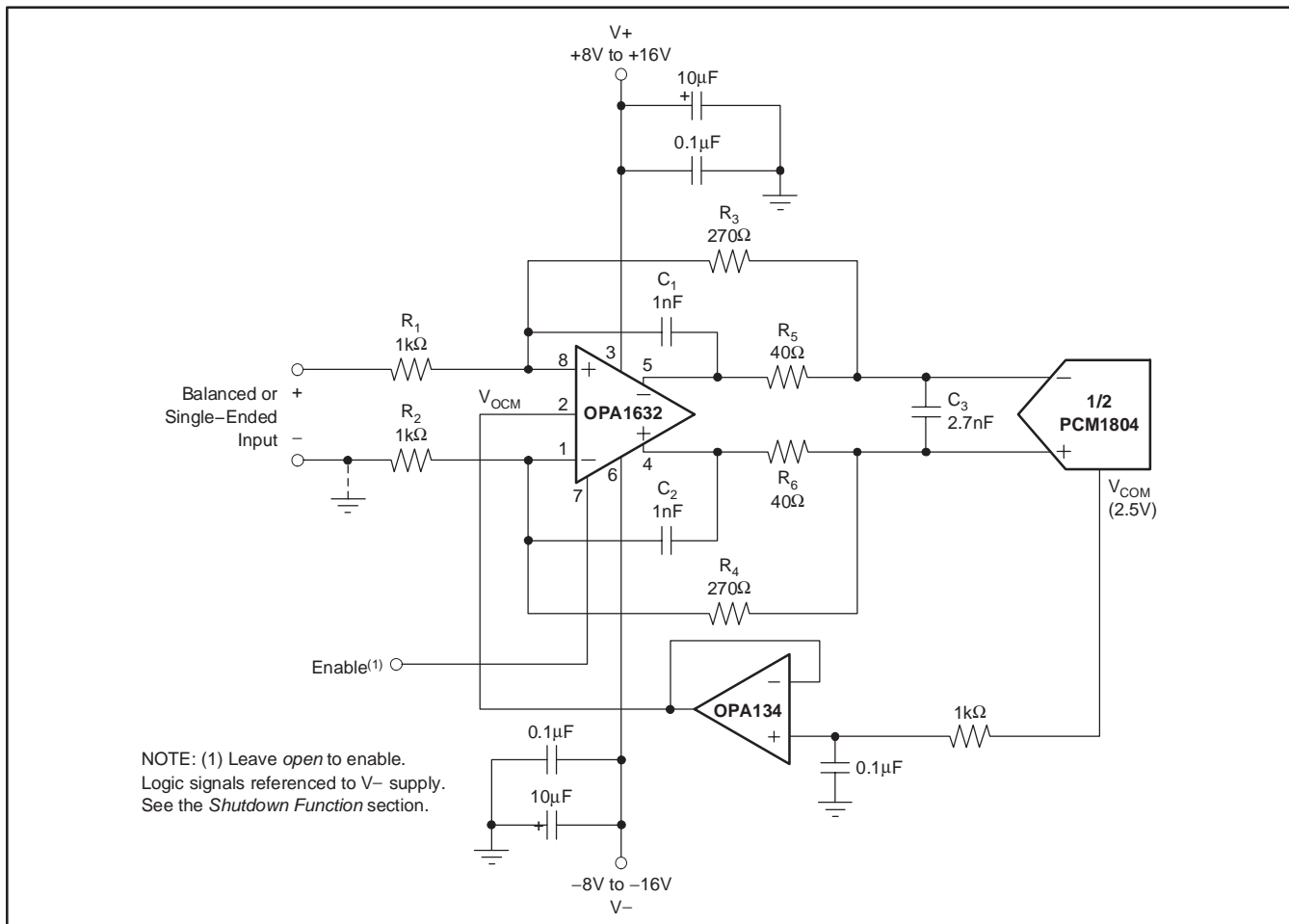


Figure 1. ADC Driver for Professional Audio

FULLY-DIFFERENTIAL AMPLIFIERS

Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. Fully-differential amplifiers not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing.

A standard configuration for the device is shown in Figure 2. The functionality of a fully differential amplifier can be imagined as two inverting amplifiers that share a common noninverting terminal (though the voltage is not necessarily fixed). For more information on the basic theory of operation for fully differential amplifiers, refer to the Texas Instruments application note SLOA054, *Fully Differential Amplifiers*, available for download from the TI web site (www.ti.com).

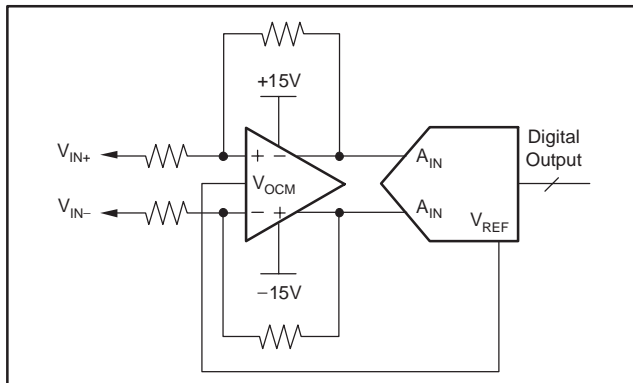


Figure 2. Typical ADC Circuit

SHUTDOWN FUNCTION

The shutdown (enable) function of the OPA1632 is referenced to the negative supply of the operational amplifier. A valid logic low ($< 0.8\text{V}$ above negative supply) applied to the enable pin (pin 7) disables the amplifier output. Voltages applied to pin 7 that are greater than 2V above the negative supply place the amplifier output in an active state, and the device is enabled. If pin 7 is left disconnected, an internal pull-up resistor enables the device. Turn-on and turn-off times are approximately $2\mu\text{s}$ each.

Quiescent current is reduced to approximately 0.85mA when the amplifier is disabled. When disabled, the output stage *is not* in a high-impedance state. Thus, the shutdown function *cannot* be used to create a multiplexed switching function in series with multiple amplifiers.

OUTPUT COMMON-MODE VOLTAGE

The output common-mode voltage pin sets the DC output voltage of the OPA1632. A voltage applied to the V_{OCM} pin from a low-impedance source can be used to directly set the output common-mode voltage. For a V_{OCM} voltage at mid-supply, make no connection to the V_{OCM} pin.

Depending on the intended application, a decoupling capacitor is recommended on the V_{OCM} node to filter any high-frequency noise that could couple into the signal path through the V_{OCM} circuitry. A $0.1\mu\text{F}$ or $1\mu\text{F}$ capacitor is generally adequate.

Output common-mode voltage causes additional current to flow in the feedback resistor network. Since this current is supplied by the output stage of the amplifier, this creates additional power dissipation. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current may be significant in some applications and may dictate use of the MSOP PowerPAD package to effectively control self-heating.

PowerPAD DESIGN CONSIDERATIONS

The OPA1632 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted (see Figure 3[a] and Figure 3[b]). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 3[c]). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

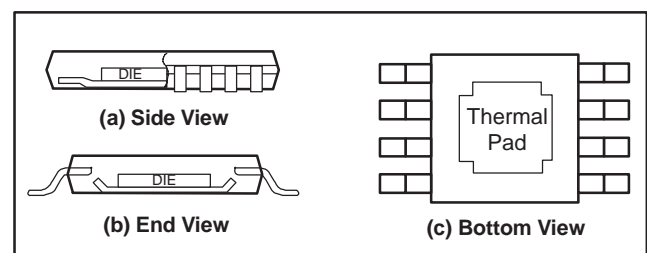


Figure 3. Views of the Thermally-Enhanced Package.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. It provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

PowerPAD PCB LAYOUT CONSIDERATIONS

1. The thermal pad must be connected to the most negative supply voltage on the device, V^- .
2. Prepare the PCB with a top-side etch pattern, as shown in Figure 4. There should be etch for the leads as well as etch for the thermal pad.

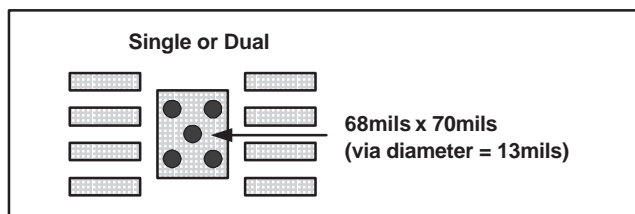


Figure 4. PowerPAD PCB Etch and Via Pattern.

3. Place five holes in the area of the thermal pad. These holes should be 13mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area.

These vias help dissipate the heat generated by the OPA1632 IC, and may be larger than the 13mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.

5. Connect all holes to the internal power plane that is at the same voltage potential as V^- .
6. When connecting these holes to the plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA1632 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal-pad area and all of the IC terminals.
9. With these preparatory steps in place, the IC is simply placed in position and runs through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The OPA1632 does not have thermal shutdown protection. Take care to assure that the maximum junction temperature is not exceeded. Excessive junction temperature can degrade performance or cause permanent damage. For best performance and reliability, assure that the junction temperature does not exceed +125°C.

The thermal characteristics of the device are dictated by the package and the circuit board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \quad (1)$$

Where:

P_{Dmax} is the maximum power dissipation in the amplifier (W).

T_{max} is the absolute maximum junction temperature (°C).

T_A is the ambient temperature (°C).

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).

θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the OPA1632 is offered in an MSOP-8 with PowerPAD. The thermal coefficient for the MSOP PowerPAD (DGN) package is substantially improved over the traditional SO package. Maximum power dissipation levels are depicted in Figure 5 for the two packages. The data for the DGN package assumes a board layout that follows the PowerPAD layout guidelines.

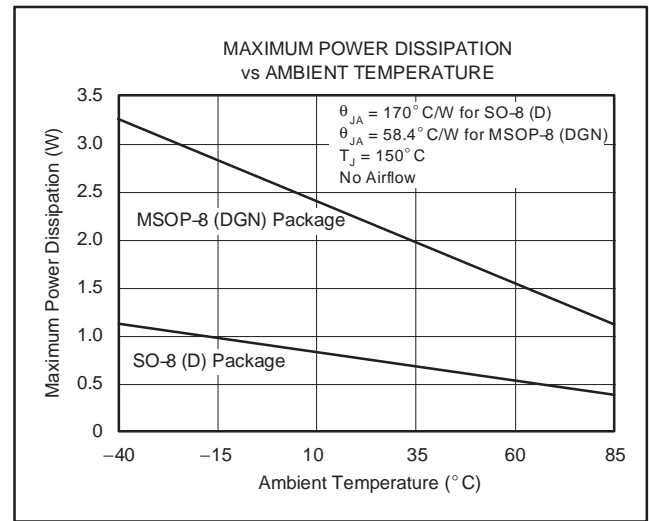


Figure 5. Maximum Power Dissipation vs Ambient Temperature

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
OPA1632D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA1632DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA1632DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA1632DGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA1632DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA1632DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA1632DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA1632DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1632DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.2	3.3	1.6	8.0	12.0	Q1
OPA1632DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



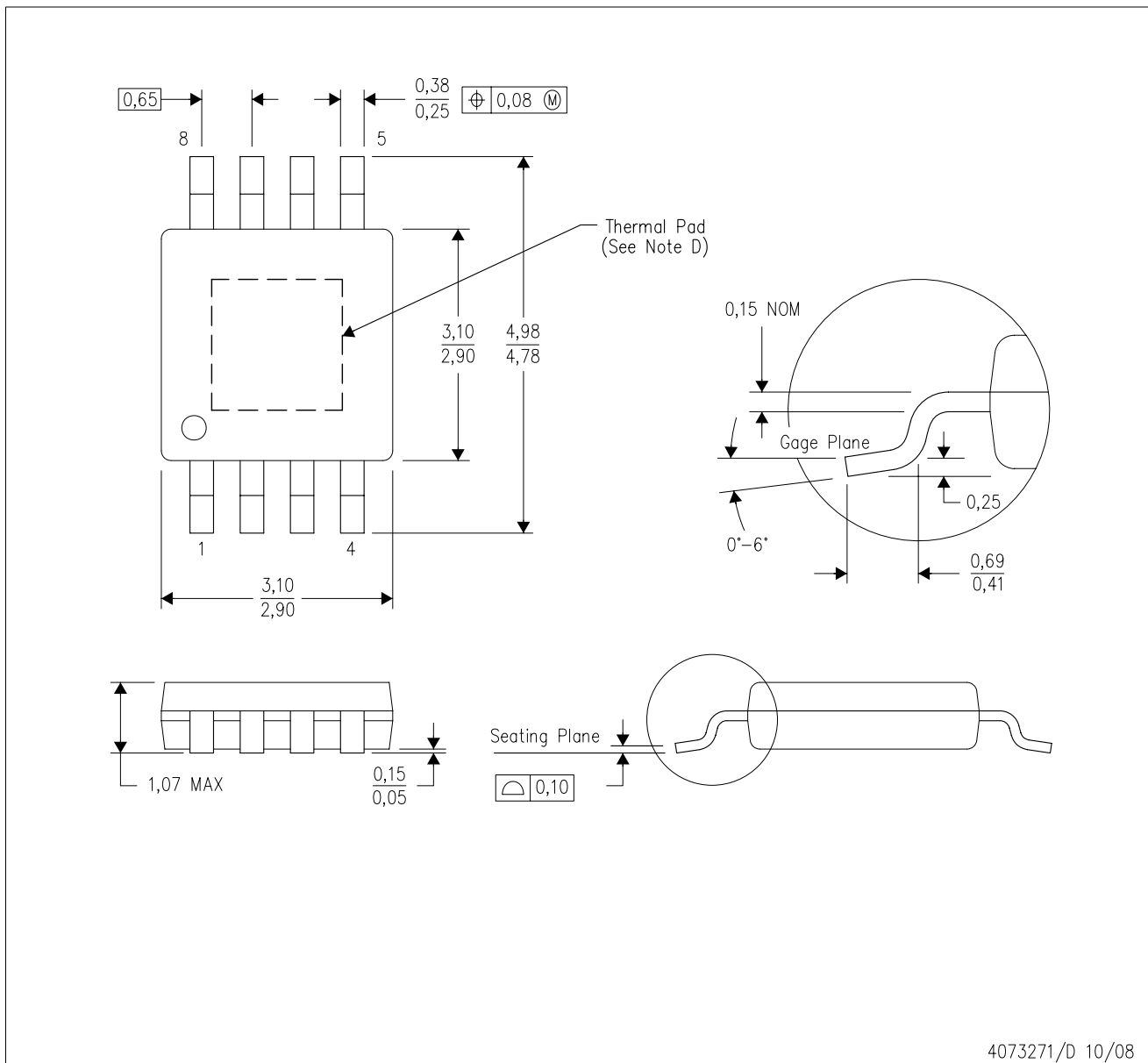
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1632DGNR	MSOP-PowerPAD	DGN	8	2500	338.1	340.5	21.1
OPA1632DR	SOIC	D	8	2500	346.0	346.0	29.0

MECHANICAL DATA

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

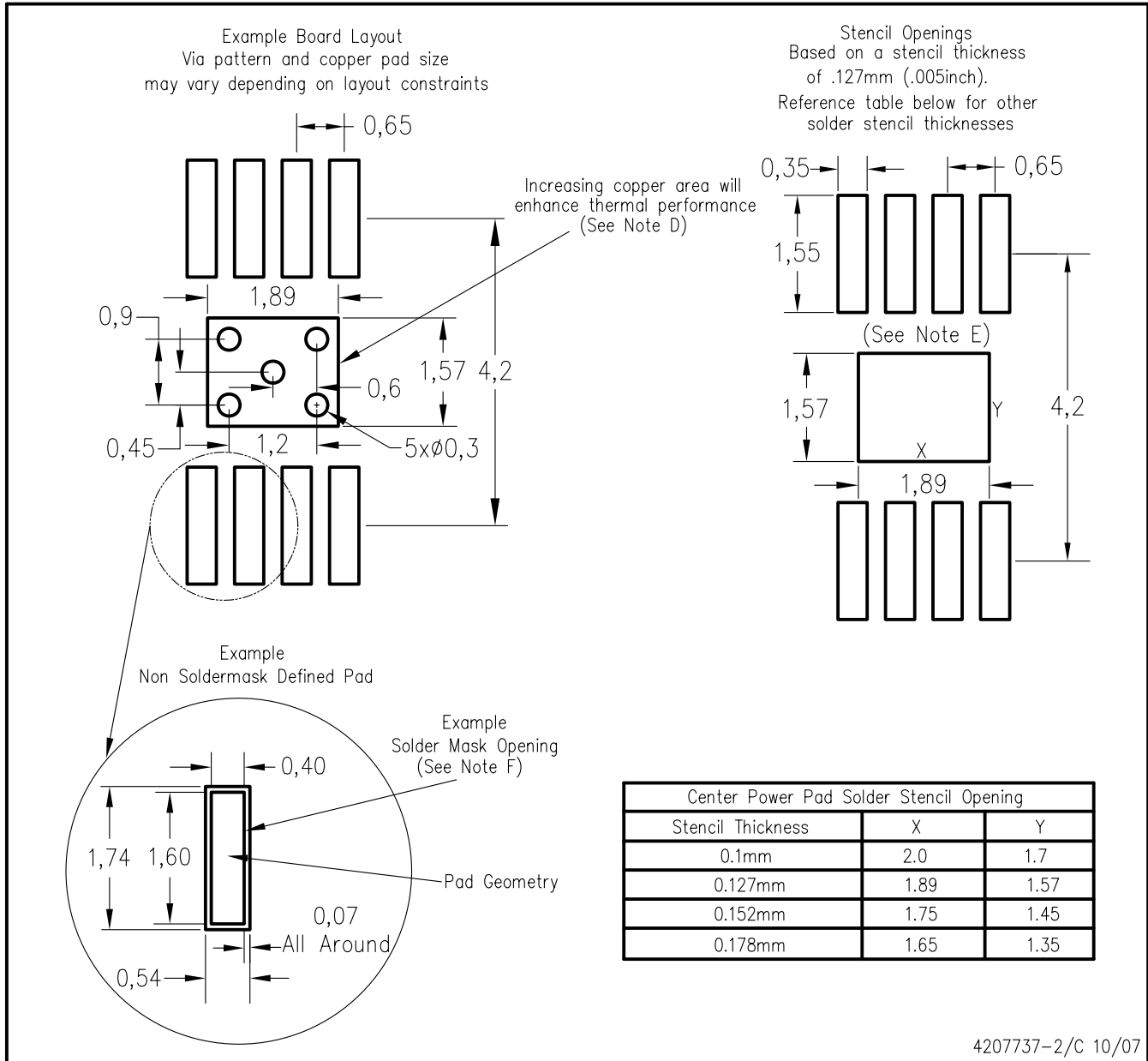
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

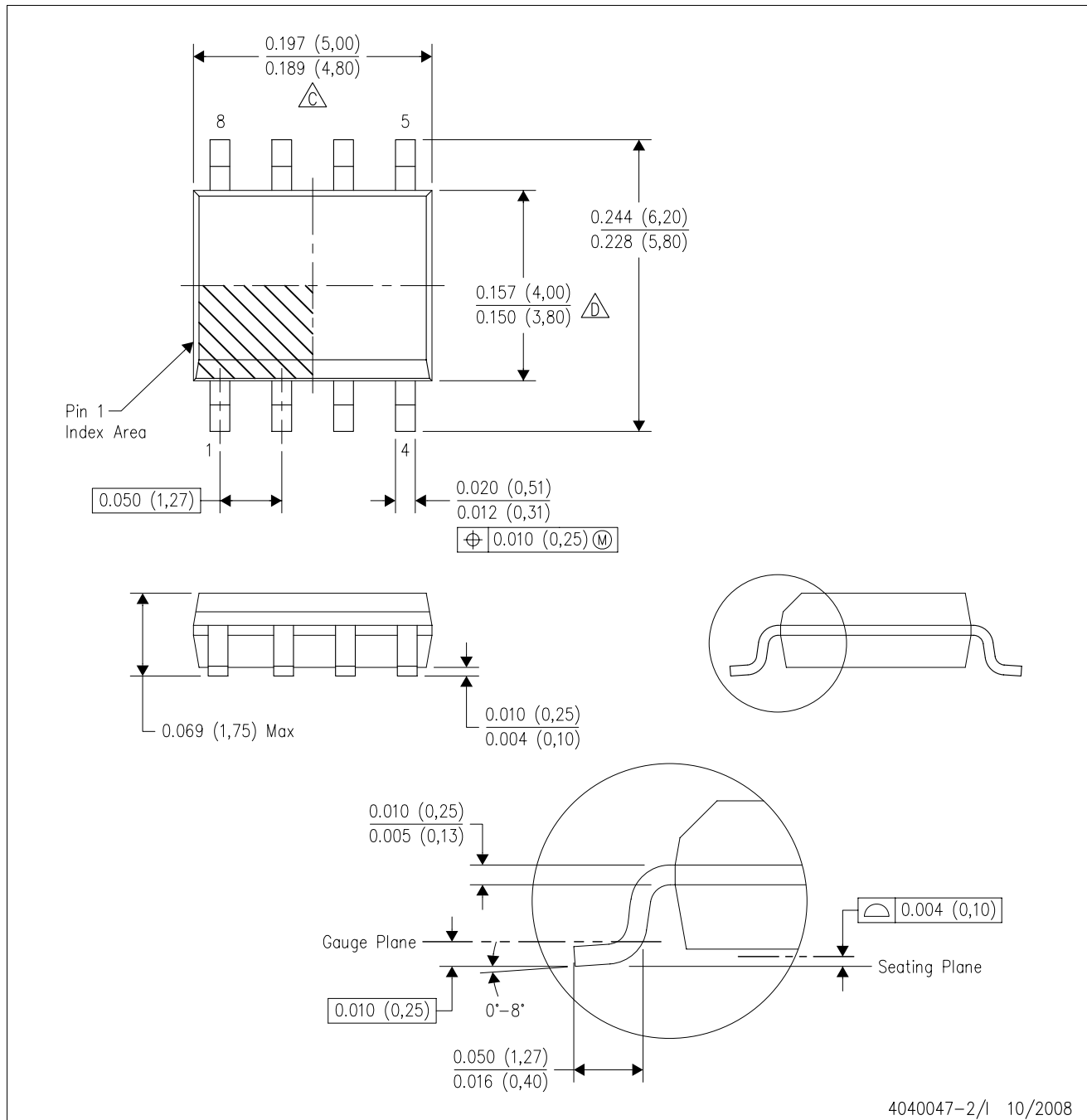
DGN (R-PDS0-G8) PowerPAD™



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated